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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/388,857	09/01/99	TRAN L	MI22-878

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EXAMINER	
SCHILLINGER,L	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 07/31/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/388,857	TRAN, LUAN C.	
	Examiner	Art Unit	
	Laura M Schillinger	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 51-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 51-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 U.S.C. § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1-7 and 51-66 are rejected under 35 U.S.C. 102(e) as being anticipated by Forbes ('351).

In reference to claim 1, Forbes teaches a method comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the regions define active areas, with some widths being no greater than 1 um, at least two being different (Fig.3 and Col.7, lines: 55-63);

forming a transistor gate line (wordline)over the active areas (Fig.4I (440) and Col.8, lines: 10-20), the transistor having different widths and voltages (Col.8, lines: 40-50).

Response to Arguments

Applicant's arguments filed 6/25/01 have been fully considered but they are not persuasive. Applicant argues that Forbes fails to teach a plurality of active areas- howeveras cited by the Examiner, Col.7, lines: 55-63 explicitly state "active areas"- in the plural sense. Applicant argues that Col.7 does not describe Fig.3- but it describes layer 300 (the active areas)- found in Fig.3.

Applicant argues extensively that Forbes Fig.4A-4F fail to depict his claim language- however the examiner did not cite Fig.s 4A-4F as aspects of Forbes's teachings which are found to be particularly relevant to the anticipation of applicant's claim language- consequently, such arguments are unpersuasive.

Applicant argues that LOCOS is not trench isolation- LOCOS (an oxide) is deposited in the shallow trenches which acts as an isolation region- the Applicant's argument asserting that the Examiner is replacing trench formation with oxide deposition techniques is unmerited.

Applicant makes an interesting argument that Forbes fails to teach "shallow trench isolation" , this inference means that Applicant argues that Forbes teaches only the formation of deep trenches. However, Forbes teaches "..in the memory cell of the invention, there are no stacked towers or DEEP TRENCHES.." (Col.11, lines: 29-30). Forbes explicitly teaches "trench isolation". Col.6, lines: 35-45 teaches that the depth of the trenches may equal to one micron or less (the width of the silicon bars). Wolf (the art cited by applicant to explain shallow trench isolation) teaches forming shallow trenches at a range between .3-.5 microns. Since Forbes teaches that the trenches

may be less than one micron- it follows that Forbes does in fact teach shallow trench isolation. Furthermore, there is no obviousness issue present.

Applicant infers that "substituting silicon bar structures for shallow trench structures in all of Applicant's independent claims gives the term "shallow trench structure" a repugnant meaning. The Examiner does not understand applicant's assertion- the Examiner never asserts substituting a silicon layer with forming a trench.

Applicant's final argument is that Forbes never mentions " width" to describe a transistor gate. However applicant's claim language never mentions "width" to describe a transistor gate-the width applicant has in his claims pertains to the width of the active regions of the transistors.

Applicant's arguments are deemed to be unpersuasive by the Examiner and consequently claim rejections are made FINAL.

In reference to claim 2, Forbes teaches wherein there is no separate channel implant (Col.7-8, lines: 64-14).

In reference to claim 3, Forbes teaches wherein the widths are less than one micron (Col.7, lines: 55-63).

In reference to claim 4, Forbes teaches wherein the threshold voltages are less than 2 volts (Col.10, lines: 35-65).

In reference to claim 5, Forbes teaches wherein the threshold voltages are less than one volt (Col.10, lines: 35-65).

In reference to claim 6, Forbes teaches wherein the widths are less than one micron and the threshold voltages are less than 2 v (Col.7, lines: 55-63 and Col.10, lines: 35-65).

In reference to claim 7, Forbes teaches wherein the widths are less than one micron and the threshold voltages are less than 1 v (Col.7, lines: 55-63 and Col.10, lines: 35-65)..

In reference to claim 51,Forbes teaches wherein one active area width is less than 1 um (Col.7, lines: 55-63).

In reference to claim 54, Forbes teaches a method comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the regions define active areas, with some widths being less than 1 um , at least two being different (Col.7, lines: 55-63);

forming a transistor gate line over the active areas (Fig.4I (440) and Col.8, lines: 10-20), the transistor having different widths and voltages (Col.8, lines: 40-50).

wherein the transistor with a lower threshold voltage has an active area with less than 1 um width (Col.7, lines: 55-63 and Col.10, lines: 35-65).

In reference to claim 55, Forbes teaches wherein the higher TV has an active area greater than 1 um (Col.7, lines: 55-63 and Col.10, lines: 35-65)...

In reference to claim 56, Forbes teaches wherein the higher TV has an active area less than 1 um (Col.7, lines: 55-63 and Col.10, lines: 35-65).

In reference to claim 57, Forbes teaches wherein one common channel implant is conducted (Col.7-8, lines: 64-14).

In reference to claim 58, Forbes teaches wherein the gate line comprises a common gate line formed over the active areas (Fig.4I (440) and Col.8, lines: 10-20).

In reference to claim 59, Forbes teaches wherein the gate line comprises a common gate line and the Ts are parallel (Fig.4I (440) and Col.8, lines: 10-20).

In reference to claim 60, Forbes teaches wherein the TV are less than 1 V(Col.10, lines: 35-65).

In reference to claim 61, Forbes teaches wherein the widths are less than 1 um, and the TV are less than 2 V (Col.7, lines: 55-63 and Col.10, lines: 35-65)..

In reference to claim 62, Forbes teaches wherein the widths are less than 1um and the TV are less than 1 V (Col.7, lines: 55-63 and Col.10, lines: 35-65)..

In reference to claim 63, Forbes teaches a method comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the regions define active areas, with some widths being less than 1 um, at least two being different (Fig. 3 and Col.7, lines: 55-63).;

forming a transistor gate line over the active areas, the transistor having different widths and voltages less than 2 V (Col.7, lines: 55-63 and Col.10, lines: 35-65)., no channel implant (Col.7-8, lines: 64-14); and

wherein the transistor with a lower threshold voltage has an active area with less than 1 um width (Col.7, lines: 55-63 and Col.10, lines: 35-65).

In reference to claim 64, Forbes teaches wherein the two widths are less than 1 um (Col.7, lines: 55-63).

In reference to claim 65, Forbes teaches wherein the TV are less than 1 v (Col.10, lines: 35-65)..

In reference to claim 66 Forbes teaches wherein the two widths are less than 1 um, and TVs are less than 1 v (Col.7, lines: 55-63 and Col.10, lines: 35-65)..

Claim Rejections - 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes ('351).

In reference to claim 52 and 53, Forbes fails to explicitly teach forming 3 transistors each have a different threshold voltage. However, it would have been obvious to one of ordinary skill in the art to fabricate additional transistors in order to create additional read/write capabilities for the memory cell which function the same way disclosed by Forbes.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication from examiner should be directed to Laura Schillinger whose telephone number is (703) 308-6425. The examiner can normally be reached by telephone on Monday to Friday from 6:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers, can be reached on (703) 308-2417. The fax phone number for the group is (703) 308-7722.

LMS

July 26, 2001

Charles Bowers
Supervisory Patent Examiner
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